ABSTRACT OF THE DISCLOSURE

A switched variable capacitor (20), and binary-weighted array (40) of such capacitors (20), are disclosed. The switched variable capacitor (20) includes a switching transistor (14) connected in series with first and second capacitors (12), between the two terminals (A,B). Bias transistors (18) are provided, and of opposite conductivity type as the switching transistor (14) but with their gates connected to the gate of the switching transistor (14). The bias transistors (18), when on, apply a reverse bias voltage to the source/drain regions of the switching transistor (14), to minimize the parasitic junction capacitance, and thus improve the temperature stability of the capacitor (20). A binary-weighted array (40) of switched variable capacitors (20) is also disclosed, as is a voltage-controlled oscillator (50) incorporating such an array (40).